What is claimed is:

1. A data register apparatus that can be loaded synchronously and unloaded out-of-phase, the apparatus comprising:

a first data register comprising a data input coupled to a data signal, a clock input coupled to a clock signal, an enable input coupled to a periodic first load signal, and a data output;

a second data register comprising a data input coupled to the data output of the first data register, a clock input coupled to the clock signal, an enable input coupled to a second load signal, and a data output; and

a controller having a clock input coupled to the clock signal, a load data input coupled to the first load signal, and a read data input coupled to a periodic read signal, the controller having a capability for generating a first guard band signal in response to the first load signal and the clock signal and a second guard band signal in response to the read signal and the clock signal, the controller further having a capability for generating the second load signal in response to the first and second guard band signals.

2. The apparatus of claim 1 wherein the second load signal is generated by performing a logical AND operation on the first and second guard band signals.

3. The apparatus of claim 1 wherein the controller has the capability for generating the first guard band signal by creating a logical low for a range of clock cycles

that begins a first predetermined quantity of clock cycles prior to the first load signal and ends a second predetermined quantity of clock cycles after the first load signal.

4. The apparatus of claim 1 wherein the controller has the capability for generating the second guard band signal by creating a logical low for a range of clock cycles that begins a first predetermined quantity of clock cycles prior to the first read signal and ends a second predetermined quantity of clock cycles after the first read signal.

5. The apparatus of claim 3 wherein the first predetermined quantity of clock cycles is substantially equal to the second predetermined quantity of clock cycles.

6. The apparatus of claim 4 wherein the first predetermined quantity of clock cycles is substantially equal to the second predetermined quantity of clock cycles.

7. The apparatus of claim 1 wherein the first data register is a "D" type flip-flop.

8. The apparatus of claim 1 wherein the second data register is a "D" type flip-flop.

9. The apparatus of claim 1 wherein the controller is a field programmable gate array.

10. A method for loading a data register apparatus synchronously with a periodic first load signal and unloading the data register apparatus out-of-phase with a read signal, the method comprising:

coupling an output of a first data register to an input of a second data register;

coupling a clock signal to a clock input of each of the first and second data registers;

generating a first guard band signal in response to the clock signal and the first load signal;

generating a second guard band signal in response to the clock signal and the read signal;

generating a second load signal in response to the first and second guard band signals; and

applying the second load signal to an enable input of the second data register.

11. The method of claim 10 wherein generating the first guard band signal comprises creating an active low signal that is low for a first predetermined quantity of clock cycles prior to the first load signal and low for a second predetermined quantity of clock cycles subsequent to the first load signal.

12. The method of claim 10 wherein generating the second guard band signal comprises creating an active low signal that is low for a first predetermined quantity of clock cycles prior to the read signal and low for a second predetermined quantity of clock cycles subsequent to the read signal.

13. The method of claim 10 wherein generating the second load signal comprises logically ANDing the first and the second guard band signals.

14. The method of claim 11 wherein the first and second quantities of clock cycles are substantially equal.

15. The method of claim 12 wherein the first and second quantities of clock cycles are substantially equal.

16. A data register apparatus that can be loaded synchronously and unloaded out-of-phase, the apparatus comprising:

a first data register comprising a data input coupled to a data signal, a clock input coupled to a periodic clock signal, an enable input coupled to a periodic first load signal, and a data output;

a second data register comprising a data input coupled to the data output of the first data register, a clock input coupled to the clock signal, an enable input coupled to a second load signal, and a data output; and

a controller having a clock input coupled to the clock signal, a load data input coupled to the first load signal, and a read data input coupled to a periodic read signal, the controller having a capability for generating a first guard band signal that has a low state a first predetermined quantity of clock cycles prior and a second predetermined quantity of clock cycles subsequent to the first load signal, the controller further having a capability for generating a second guard band signal that has a low state a third

predetermined quantity of clock cycles prior and a fourth predetermined quantity of clock cycles subsequent to the read signal, the controller further having a capability for generating the second load signal by performing a logical AND operation on the first and second guard band signals.

17. The apparatus of claim 16 wherein the first and second guard bands are periodic.

18. In a controller, a method for loading a data register apparatus synchronously with a periodic first load signal and unloading the data register apparatus out-of-phase with a read signal, the apparatus comprising a first data register having an output coupled to an input of a second data register, both data registers being clock by a periodic clock signal, the method comprising:

generating a first guard band signal that is low for a first predetermined quantity of clock cycles prior and a second predetermined quantity of clock cycles subsequent to the first load signal;

generating a second guard band signal that is low for a third predetermined quantity of clock cycles prior and a fourth predetermined quantity of clock cycles subsequent to the read signal; and

generating a second load signal by logically ANDing the first and second guard band signals.

19. The method of claim 18 and further including coupling the second load signal to an enable input of the second data register.

20. The method of claim 18 wherein the controller is a field programmable gate array.